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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,692	09/29/2003	Kyle K. Kirby	2269-5665US (02-1291.00/U	4168

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EXAMINER	
ESTRADA, MICHELLE	
ART UNIT	**PAPER NUMBER**
2823	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,692	KIRBY, KYLE K.	
	Examiner	Art Unit	
	Michelle Estrada	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,11,12,14-16,22,23 and 28* is/are rejected.

7)☒ Claim(s) *3,7-10,13,17-21 and 24-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4-6, 11, 12, 14-16, 22-23 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Wood et al. (6,773,938).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Re claim 1, Wood et al. disclose providing a semiconductor substrate (200); ablating one or more depressions (210) in a surface of the semiconductor substrate to define the at least one electrical pathway, the depressions extending along the surface (See fig. 5); depositing an electrically conductive material (220) over the surface of the semiconductor substrate and into the one or more depressions (Fig. 7); and planarizing the electrically conductive material at least to the surface of the semiconductor

substrate to laterally isolate the electrically conductive material in the one or more depressions (Fig. 8).

Re claim 4, Wood et al. disclose wherein providing the semiconductor substrate comprises providing a silicon wafer (200) (Col. 3, lines 58-62).

Re claim 5, Wood et al. disclose wherein depositing the electrically conductive material (220) over the surface of the semiconductor substrate comprises depositing a metal (Col. 5, lines 25-30).

Re claim 6, Wood et al. disclose wherein depositing the at least on of the metal over the surface of the semiconductor substrate comprises depositing a metal selected from the group consisting of aluminum, nickel, copper, gold and alloys therof over the semiconductor substrate.

Re claim 11, Wood et al. in view of Patterson et al. as explained above, disclose providing a semiconductor substrate (200); and substantially simultaneously ablating one depression (210) in a surface of the semiconductor substrate to define the at least one conductive element in the form of an elongated trace, the at least one depression extending along the surface of the semiconductor substrate, and ablating at least one conductive structure precursor in the semiconductor substrate comprising a via (210) extending into the semiconductor substrate transverse to the surface to define the at least one conductive structure (See fig. 2d).

Re claim 12, Wood et al. disclose depositing an electrically conductive material (220) over the surface of the semiconductor substrate and into the at least one depression and the at least another depression; and planarizing the electrically

conductive material at least to the surface of the semiconductor substrate to laterally isolate the electrically conductive material in the at least one depression and the at least another depression.

Re claim 14, Wood et al. disclose wherein providing the semiconductor substrate comprises providing a silicon wafer (200) (Col. 3, lines 58-62).

Re claim 15, Wood et al. disclose wherein depositing the electrically conductive material (220) over the surface of the semiconductor substrate comprises depositing a metal (Col. 5, lines 25-30).

Re claim 16, Wood et al. disclose wherein depositing the at least on of the metal over the surface of the semiconductor substrate comprises depositing a metal selected from the group consisting of aluminum, nickel, copper, gold and alloys thereof over the semiconductor substrate.

Re claim 22, Wood et al. disclose providing a semiconductor substrate (200) having an active surface, a backside surface, and at least one sidewall oriented substantially perpendicular to the active surface and the backside surface; and ablating one or more depressions (210) in a surface of a sidewall of the semiconductor substrate to define the at least one electrical connection.

Re claim 23, Wood et al. disclose depositing an electrically conductive material (220) over the surface of the semiconductor substrate and into the one or more depressions; and planarizing the electrically conductive material at least to the surface of the semiconductor substrate to laterally isolate the electrically conductive material in the one or more depressions.

Re claim 28, Wood et al. disclose providing a laser configured to emit a laser beam; and traversing the surface of the semiconductor substrate with the laser beam.

Allowable Subject Matter

Claims 3, 7, 8, 9, 10, 13, 17-21 and 24-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 11/16/06 have been fully considered but they are not persuasive. Applicant argues that Wood et al. does not describe "ablating one or more depressions *in and along a surface* of the semiconductor substrate to define at least one electrical pathway *extending along the surface*", and further Applicant argues that Wood et al. disclose that the holes 210 extend inwardly. However, holes 210 extend inwardly and along the surface of the semiconductor substrate. Holes 210 of Wood et al. while extending inwardly still extend along the surface too. If Applicant intends any particular extension along the surface, it must be clearly recited.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle Estrada whose telephone number is 571-272-1858. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2800.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michelle Estrada
Primary Examiner
Art Unit 2823

ME
February 6, 2007